REMARKS

Claims 4-13 are pending in the present application. Claim 4 has been amended. Claims 5-13 have been presented herewith.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document in parent application Serial No. 09/584,549.

Drawings

Applicant notes the Examiner's acceptance of the drawings as filed along with the present application on January 29, 2004.

Disclosure

The disclosure has been objected to in view of the informality as listed on page 2 of the current Office Action dated May 22, 2006. The Cross Reference to Related Applications paragraph has thus been corrected to update the status of parent application Serial No. 09/584,549, as abandoned. The Examiner is therefore respectfully requested to withdraw this objection.

Claim Rejections-35 U.S.C. 102(b)

Claim 4 has been rejected under 35 U.S.C. 102(b) as being clearly anticipated by the Takamuki reference (U.S. Patent No. 6,021,420). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The transposition circuit of claim 4 includes in combination among other features "wherein the transposition circuit is provided with N memory units having storage areas to accommodate N data packets, N input selectors having output ports individually connected to input ports of the memory units, N output selectors having output ports individually connected to said output terminals, and a control unit...wherein said input and output selectors having N ports, and any of the ports of said input and output selectors are used as an input port in accordance with a common selection signal from said control unit to said input and output selectors...and wherein said control unit generates the common selection signal, and produces address signals to specify a common storage area for each of the memory units, to both read data from and write data to the common storage areas during a same period". Applicant respectfully submits that the Takamuki reference as relied upon does not disclose these features.

As described generally in column 5, lines 19-20 of the Takamuki reference, the reading procedure is executed **after** the writing procedure. The writing procedure is more generally described in column 5, lines 22-39 of the Takamuki reference, and the reading procedure is more generally described in column 5, lines 40-59. The writing procedure is more specifically described beginning in column 6, line 50 with respect to

Figs. 3A – 3C of the Takamuki reference. The read operation is subsequently described beginning in column 7, line 1 of the Takamuki reference with respect to Figs. 3D – 3F. It should thus be readily clear that the device of the Takamuki reference does not both read data from and write data to common storage areas during a same period, as would be necessary to meet the features of claim 4. Applicant therefore respectfully submits that the transposition circuit of claim 4 distinguishes over the Takamuki reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 4, is improper for at least these reasons.

With further regard to this rejection, as described in column 4, lines 50-55 of the Takamuki reference with respect to Fig. 2, when storing input column vectors, or in other words when writing data into the storage devices 22, control device 25 outputs first control signal CTL1 to input selection devices 21 and at the same time outputs second control signal CTL2 to the address generators 23. On the other hand, as further described in column 4, lines 61-65 of the Takamuki reference with respect to Fig. 2, when reading data stored in the storage devices 22, control device 25 outputs second control signal CTL2 to the address generators 23 and at the same time outputs third control signal CTL3 to the output selection devices 24. Thus, it should be readily understood that the input selection devices 21 and the output selection devices 24 in Fig. 2 of the Takamuki reference do not provide outputs responsive to a common selection signal, as would be necessary to meet the features of claim 4. Applicant therefore respectfully submits that the transposition circuit of claim 4 distinguishes over

the Takamuki reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to currently pending claim 4, is improper for at least these reasons.

Claims 5-13

Applicant respectfully submits that claims 5-10 distinguish over the Takamuki reference as relied upon by the Examiner at least by virtue of dependency upon claim 4, and by further reason of the features therein.

The transposition circuit of claim 11 includes in combination among other features a controller "that provides the common selection signal, and that provides address signals to the N memory units to designate common storage areas, wherein data is both written into and read out from the common storage areas during a same period".

Applicant respectfully submits that the Takamuki reference as relied upon does not disclose a common selection signal, and does not provide a device wherein data is both written into and read out from common storage areas during a same period, as would be necessary to meet the features of claim 11. Applicant therefore respectfully submits that claims 11-13 distinguish over the Takamuki reference as relied upon for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the

corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

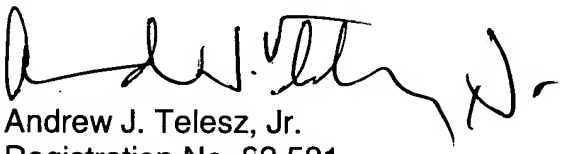
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of three (3) months to November 22, 2006, for the period in which to file a response to the outstanding Office Action. The required fee of $1020.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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